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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

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Application Number	Filed
10/537,857	Apr. 3, 2005

First Named Inventor: SHAPPIR, Assaf

Art Unit	Examiner
2824	NGUYEN, Dang T.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3 73(b) is enclosed (Form PTO/SB/96)
- ☒ attorney or agent of record Registration number 43,116
- ☐ attorney or agent acting under 37 CFR 1 34 Registration number if acting under 37 CFR 1 34 _____

Signature

Vladimir Sherman
Typed or printed name

212 608 4141
Telephone number

December 10, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted

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Attorney Docket No.: P-6715-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Assaf Shappir	Examiner:	Nguyen, Dang T
Serial No.:	10/537,857	Group Art Unit:	2824
Filed:	06/07/2005		
Title:	Method, circuit and system for erasing one or more non-volatile memory cells		

ARGUMENTS SUBMITTED IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

This communication is filed with and in support of a Pre-Appeal Brief Request for Review, requesting a panel review to determine whether the Examiner has established a prima facie case of anticipation with respect to pending claims 1-19. It is the Applicant's position that:

The Examiner Appears to have misinterpreted the teachings of the Chindalore reference and misapplied teachings of Chindalore which in fact contradicted the recited limitations of independent claims 1, 9 and 19. More specifically, the Examiner appears to have confused an "erase pulse" with a "voltage threshold", and continues to insist that a non-flat voltage threshold is the same a non-flat erase pulse. Whereas all the independent claims of the pending application recite "**an erase pulse having a substantially non-flat voltage profile**", the cited reference teaches a ***threshold voltage*** profile which is non-flat due to multiple erase cycles. In other words, the cited reference teaches a non-flat threshold voltage profile of a memory cell programming or erasure procedure, which consists of **numerous flat** erase/program **pulses/cycles**, while the independent claims of the present Application recite a non-flat voltage of an **erase pulse itself**.

The pending independent claims recite:

1. "A method of erasing one or more non-volatile memory ("NVM") cells comprising: applying to the one or more NVM cells **an erase pulse having a substantially non-flat voltage profile**."

9. "A circuit for erasing one or more non-volatile memory ("NVM") cells comprising: an erase pulse source to produce **an erase pulse having a substantially non-flat voltage profile**."

19. "A system for erasing one or more non-volatile memory ("NVM") cells comprising: A NVM array, and an erase pulse source to produce **an erase pulse having a substantially non-flat voltage profile**."

As clear from the reading of claims 1, 9 and 19, according to the claimed invention, the erase process comprises applying "...**an erase pulse having a substantially non-flat voltage profile**...", or in other words, **the erase pulse itself is non flat and the voltage is changed within the same [[single]] pulse.**

The portions of Chindalore to which the Examiner points in support of his anticipatory rejections of claims 1, 9 and 19 describe the **result** of the claimed limitation within the rejected claims. More specifically, Column 3, lines 19-23, fig. 2 and column 5 lines 5-7 of the Chindalore reference, which the Examiner stated teach emphasized limitation of independent claims 1, 9 and 19, respectively recite:

"As the program/erase threshold voltage changes with the number of program/erase cycles, a variable read reference cell gate voltage 26 changes, thus maintaining an optimum voltage margin 28 between the program threshold voltage and the erase threshold voltage."

"The resulting cell voltage V.sub.CELL increases over time as the memory is programmed and erased, as illustrated in FIG. 2."

As shown above, the cited reference only teaches a ***threshold voltage*** profile which is non-flat due to multiple erase cycles. As one of ordinary skill in the art should know, a threshold voltage profile is a function of program or erase pulses, it is not the pulse itself. Applicant respectfully asserts that the Examiner has misinterpreted the teachings of the cited reference, by drawing an analogy between the change in **threshold voltage** along numerous **erase cycles**, as taught in the cited reference, and the application of a non-flat **erase pulse**, recited in the pending claims and application.

Furthermore, regarding the second section of the cited reference quoted above, the Applicant would like to point out to the panel the context in which it is brought, as follows:

"As shown in FIG. 1 and FIG. 2, ***as the number of program and erase operations increase, the program and erase threshold voltage of the memory cells increase.*** Because reference transistor 46 is undergoing the same program and erase operations as memory array 32, its threshold voltage will also increase, causing reference current i.sub.REF to decrease by a corresponding amount. During a read operation, reference current i.sub.REF is fed back to voltage control circuit 48. Voltage control 48 will adjust the gate voltage V.sub.REF of reference transistor 46 and cell voltage V.sub.CELL as a function of the decreasing reference current. *The resulting cell voltage V.sub.CELL increases over time as the memory is programmed and erased, as illustrated in FIG. 2.*"

It would appear the Examiner has stubbornly and repeatedly cited bits and pieces of the cited reference in support of his erroneous argument without actually looking into their meaning. The cited reference teaches a non-flat threshold voltage profile which may be the result of multiple pulses, where consecutive pulses may be at different voltages, but where each individual pulse has a substantially flat profile.

Additionally, figures 1 and 2 of the cited reference, clearly teach a ***threshold voltage*** profile which is non-flat ***due to multiple erase cycles***, whereas independent claims 1, 9 and 19 of the present Application clearly recite "...**an erase pulse having a substantially non-flat voltage profile**...".

Applicant respectfully asserts that the difference between ***threshold voltage*** profile which is non-flat ***due to multiple erase cycles***, as taught in the cited reference, and **an erase pulse having a substantially non-flat voltage profile**, as recited in independent claims 1, 9 and 19 of the present Application, should be entirely clear to one of ordinary skill in the art.

In view of the foregoing remarks, all pending claims are considered to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Respectfully submitted,

Vladimir Sherman
Attorney for Applicant(s)
Registration No. 43,116

Dated: October 11, 2007

EMPK & Shiloh, LLP
116 John St, Suite 1201
New York, NY 10038
General Phone:(212) 608-4141
Facsimile: (212) 608-4144